REMARKS

Claims 1-30 are pending herein with claims 7-30 having been added herein. Claims 1-4 and 6 have also been amended herein. In view of this amendment reconsideration are hereby requested.

Applicant wishes to thank the Examiner for the indication of allowable subject matter in claim 6.

The oath or declaration has been objected to as being defective because non-dated alterations have been made to the residence and post office address and because the second inventor did not date the document. A new declaration has been executed and is included herewith.

The drawings have been objected to because Figure 2 has a mislabeled transistor and is not consistent with the specification and claims. The drawing has been corrected. Claim 2 has also been amended to be more consistent with the illustration. This amendment does not narrow the claim. Figure 1 has also been amended to be more consistent with the specification. It is respectfully submitted that the drawings are in compliance with the rules.

The specification has been amended to correct typographical errors. The abstract has also been replaced. This new abstract is within the word limit and complies with the rules. A clean copy of the abstract has been provided on a separate sheet.

Claims 1, 3, and 6 have been objected to in view of formalities. These formalities have been clarified as suggested by the Examiner. None of the clarifications narrows the scope of any claim term.

Claims 1-6 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Applicant respectfully submits that the claims, as amended, fully comply with Section 112.

Claim 1 was rejected for being incomplete for omitting essential structural cooperative relationships of elements. In response, claim 1 has been amended to specifically recite that the enable/disable section is coupled to the level shifting section. This clarification provides structural cooperative relationships of the elements and therefore the claim is definite.

A number of rejections related to the sentences provided from lines 10-15. These rejections, however, are moot in view of the cancellation of these sentences. Claims 7 and 8 have been added herein to specifically claim the elements provided in those canceled sentences.

Claims 2 and 4 have been amended to more clearly recite the claimed subject matter. These amendments do not narrow the scope of the claims.

Claim 1 has been rejected under 35 U.S.C. 102(b) as being anticipated by Stewart (U.S. Patent No. 4,216,390) and claims 2-5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Stewart. Applicant respectfully traverses this rejection.

Applicant respectfully submits that claims 1-5, as originally filed, are allowable over Stewart. For example, claim 1 recites that "the enable/disable section plac[es] the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode." It is respectfully submitted that Stewart does not teach or suggest the limitations of claim 1.

In reviewing the Stewart reference, the Examiner stated that "an enable/disable section 16 [is] responsive to an enable/disable signal Vc for placing the output terminal 30 to a high output impedance condition (when transistor P3 is OFF) independent of the logic state of the input signal during disable mode." Applicant respectfully submits that this statement is simply

incorrect. Control circuit 16 is for selectively changing the operating potential applied to latch 12. Stewart, col. 1, lines 44-45. As explained by the reference, "[w]hen Vc is at V3, P3 is turned-off and V2 volts are coupled to node 34 via D2." Col. 2, lines 23-24. The reference does not teach any condition where the terminal 30 is placed at a relatively high output impedance condition. Therefore, it is respectfully submitted that claim 1 is allowable over Stewart.

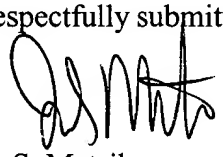
Claims 2-5 and 7-8 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding further limitations.

Claim 6 has been amended herein to be placed in independent form by including the limitations of claims 1-4. The Examiner has indicated that this claim is allowable.

Claims 9-30 have been added herein to more comprehensively claim the present invention. No new matter has been added. Applicant respectfully submits that claims 9-30 are allowable over the references of record.

In view of the above, Applicant respectfully requests withdrawal of the Examiner's rejection and allowance of the pending claims. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's agent at the below listed telephone number and address.

Respectfully submitted,



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Appendix I

Marked Version of Specification

Page 4, paragraph 2, lines 9-30:

More particularly, the level-shifting section 12 includes an input transistor N_1 having a control, here gate, electrode coupled to a +2.1 volt supply, a first electrode coupled to the input logic signal IN, and a second electrode. An output pair of serially coupled complementary type transistors, i.e., P type MOSFET P_2 and N type MOSFET N_2, is provided. A first one of the pair of transistors P_2 has a first electrode coupled to a source, not shown, of the third voltage level (+2.5 volts) through a first switching transistor P type MOSFET P_3 and a control electrode coupled to the second electrode of the input transistor N_1. A junction 16 between the output pair of transistors P_2, N_2 provides the output terminal OUT for the level-shifting circuitry 10. A control electrode of the second one of the pair of transistors N_2 is connected to the first electrode of the input transistor N_1. The second one of the pair of transistors N_2 has a second electrode coupled to the second voltage level, here ground, through a second switching transistor N_3. The first and second switching transistors P-type MOSFET P_3 and N-Type MOSFET[s] N_3 are fed by the enable/disable signal ENABLE, the transistor P_3 bein[b]g coupled to the enable/disable signal ENABLE via an inverter 18, as shown. The level-shifting section 12 includes an additional transistor P type MOSFET P_1. The additional transistor P_1 has a control electrode connected to the junction 16, a first electrode coupled to the source of the third voltage level +2.5 through the first switching transistor P_3 and a second electrode connected to the second electrode of the input transistor N_1. The input transistor N_1 and the additional transistor P_1 are of

opposite conductivity type. The enable/disable circuit 14 includes an inverter 18 fed by the enable/disable signal ENABLE. The inverter 18 having an output coupled to the control electrode of the first switching transistor P_3.

Appendix II

Marked Version of Claims

1. Level shifting circuitry, comprising:

a level-shifting section responsive to an input logic signal, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state, such level-shifting section providing an output logic signal at an output terminal thereof having a third voltage level representative of the first logic state of the input logic signal and a fourth voltage level representative of the second logic state of the input signal;

an enable/disable section coupled to the level shifting section, the enable/disable section being responsive to an enable/disable signal, [for] the enable/disable section placing the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode.

[In one embodiment, the level-shifting section includes an additional transistor. The additional transistor has a control electrode connected to the junction, a first electrode coupled to the source of the third voltage level through the first switching transistor and a second electrode connected to the second electrode of the input transistor. In one embodiment, the input transistor and the additional transistor are of opposite conductivity type.]

2. The level shifting circuitry recited in claim 1, wherein the level-shifting [section] circuitry includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

a first switching transistor;

a second switching transistor;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the level-shifting circuitry, a control electrode of the second one of the pair of transistors being connected to the [first] second electrode of the input transistor, the second one of the pair of transistors having a second electrode coupled to the second voltage level through the second switching transistor; and

wherein the first and second switching transistors are fed by the enable/disable signal.

3. The level shifting circuitry recited in claim 2 wherein the enable/disable [circuit] section includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor.

4. The level shifting circuitry recited in claim 3 wherein the inverter is powered by a voltage source [of] held at the first voltage level.

6. [The l]Level shifting circuitry [recited in claim 4,] comprising:

a level-shifting section responsive to an input logic signal, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state, such level-shifting section providing an output logic signal at an output

terminal thereof having a third voltage level representative of the first logic state of the input logic signal;

an enable/disable section coupled to the output terminal, the enable/disable section being responsive to an enable/disable signal, the enable/disable section placing the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode, the enable/disable section including a first switching transistor and a second switching transistor;

wherein the level-shifting section includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the level-shifting circuitry, a control electrode of the second one of the pair of transistors being connected to the second electrode of the input transistor, the second one of the pair of transistors having a second electrode coupled to the second voltage level through the second switching transistor;

wherein the first and second switching transistors are fed by the enable/disable signal;

wherein the enable/disable section includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor;

wherein the inverter is powered by a source of the first voltage level; and

wherein the inverter comprises [:] a level shifter for shifting the level of the enable/disable signal from the first voltage level to the third voltage level and for feeding such third voltage level to the control electrode of the first switching transistor to [placing] place the first switching transistor to a non-conducting condition during the disable mode.

Formals
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FIG. 1
(PRIOR ART)

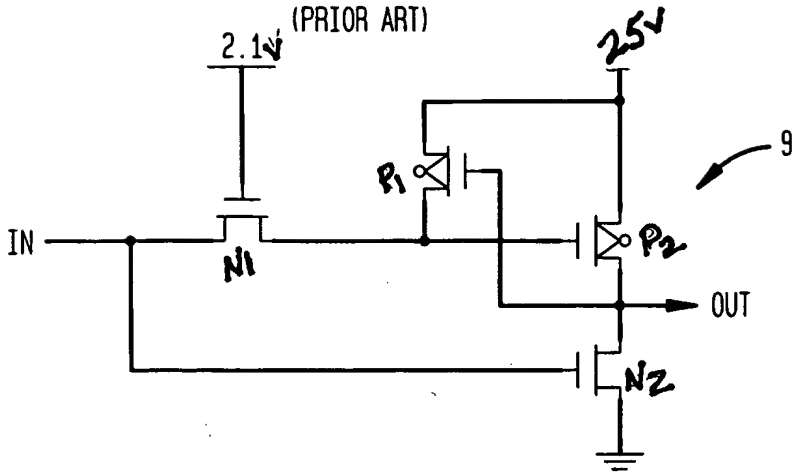

FIG. 2